AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (canceled) A method of recovering a network timing clock of a service input of a packet-based telecommunications network, comprising the steps of:

receiving an external clock reference from a source node as an input;

providing an external clock with a frequency reference value;

dividing the external clock reference input by an integer;

configuring a status register depending on the value of the external clock frequency;

generating an integer value at the status register;

providing a divider for the generated value of the status register;

providing a digital phase locked loop to lock onto the external reference clock

2. (canceled) The method of claim 1, wherein the integer that divides the external clock value is N.

3. (canceled) The method of claim 1, wherein the integer value generated at the status register is Y.

4. (canceled) The method of claim 1, wherein digital phase locked loop compares the external reference clock and a locally generated reference clock to produce an output reference clock.

5. (canceled) The method of claim 1, wherein a numerically controlled oscillator is used to generate the local reference clock.

6. (canceled) An apparatus for recovering a network timing clock of a service input of a packet-based telecommunications network, comprising the steps of:

a receiver for receiving an external clock reference from a source node as an input;

a divider for dividing the external clock reference input by an integer;

a status register to be configured depending on the value of the external clock frequency;

a generator that generates an integer value at the status register;

a divider for dividing the generated value of the status register;

a digital phase locked loop that locks onto the external reference clock

7. (canceled) The apparatus of claim 6, wherein the integer that divides the external clock value is N.

8. (canceled) The apparatus of claim 6, wherein the integer value generated at the status register is Y.

9. (canceled) The apparatus of claim 6, wherein digital phase locked loop compares the external reference clock and a locally generated reference clock to produce an output reference clock.

10. (canceled) The apparatus of claim 6, wherein a numerically controlled oscillator is used to generate the local reference clock.

11. (new) A method of recovering a network timing clock of a service input for a packet-based telecommunications network, comprising the steps of:

receiving an external clock reference signal from a source node as an input;

generating a first integer and a second integer at a configuration and status register;

inputting one generated integer into a first divider, and the other generated integer into a second divider;

inputting the received external clock reference signal into the first divider;

inputting a high speed bus clock signal into the second divider;

dividing the received external clock reference signal by the first integer to produce a divided external clock reference;

dividing the high speed bus clock signal by the second integer to produce an internal clock reference signal;

inputting the first divider output and the second divider output into an arithmetic logic unit to produce a reference clock signal;

inputting the reference clock signal into a digital phase-locked loop;

providing the digital phase locked loop to lock onto the external reference clock.

12. (new) The method of claim 11, wherein the first integer that divides the external clock value is N_1, which is selected to be either 1, 256, 193 or 192.

13. (new) The method of claim 12, wherein the value of N_1 of the first divider is selected depending on an external clock frequency, in order to generate an 8 KHz local frequency.

14. (new) The method of claim 13, wherein the external clock frequency maybe 8 KHz, 2.048 MHz, 1.536 MHz or 1.544 MHz.

15. (new) The method of claim 11, wherein the second integer value generated at the status register is Y_1.

16. (new) The method of claim 11, wherein the value of Y_1 of the second divider is selected in order to divide the inputted high-speed clock signal to produce a local 8 KHz frequency.

17. (new) The method of claim 11, wherein the digital phase locked loop further comprises a numerically-controlled oscillator, a fourth divider, a phase comparator and a low-pass filter for producing a locally generated reference clock signal.

18. (new) The method of claim 11, wherein a selection mode is implemented to choose the local 8 KHz frequency from the first or the second divider as a reference for a phase comparator.

19. (new) The method of claim 15, wherein the numerically-controlled oscillator is implemented as third divider that is a $Y_2/2^{N}{}_2$ that receives the high speed bus clock signal.

20. (new) The method of claim 15, wherein the fourth divider is implemented as a $1/N_3$ divider that receives the output of the numerically controlled oscillator to produce a locally generated reference signal.

21. (new) The method of claim 15, wherein phase comparator compares a time delay between rising edges of the external reference clock and a locally generated reference clock to determine a phase error as a correction factor to modify the value of Y_2.

22. (new) The method of claim 17, wherein the value of N_3 in the $1/N_3$ divider is chosen from a group of integers including 256, 193 or 192 depending on the numerically-controlled oscillator clock output.

23. (new) The method of claim 19, wherein the value of Y_2 is increased, when the external reference clock frequency edge occurs before the locally generated reference clock frequency edge.

24. (new) The method of claim 19, wherein the value of Y_2 is decreased, when the external reference clock frequency edge occurs after the locally generated reference clock frequency edge.

25. (new) The method of claim 21, wherein the value of Y_2 is increased by an amount proportional to the difference in time between the external reference clock frequency edge and the locally generated reference clock frequency edge.

26. (new) The method of claim 22, wherein the value of Y_2 is decreased by an amount proportional to the difference in time between the external reference clock frequency edge and the locally generated reference clock frequency edge.

27. (new) An apparatus for recovering a network timing clock of a service input for a packet-based telecommunications network, comprising:

a receiver for receiving an external clock reference signal from a source node as an input;

a configuration and status register generating for generating a first integer and a second integer;

a first divider for receiving the first generated integer and received external clock reference signal, and a second divider for receiving the second generated integer and a high speed bus clock signal;

dividing the received external clock reference signal by the first integer to produce a divided external clock reference;

an arithmetic logic unit for receiving the outputs of the first divider and the second divider to produce a reference clock signal;

a digital phase-locked loop for receiving the reference clock signal to lock onto the external reference clock.

28. (new) The apparatus of claim 27, wherein the first integer that divides the external clock value is N_1, which is selected to be either 1, 256, 193 or 192.

29. (new) The apparatus of claim 28, wherein the value of N_1 is selected depending on an external clock frequency, in order to generate an 8 KHz local frequency.

30. (new) The apparatus of claim 29, wherein the external clock frequency maybe 8 KHz, 2.048 MHz, 1.536 MHz or 1.544 MHz.

31. (new) The apparatus of claim 27, wherein the second integer value generated at the status register is Y_1.

32. (new) The apparatus of claim 27, wherein the value of Y_1 of the second divider is selected in order to divide the inputted high-speed clock signal to produce a local 8 KHz frequency.

33. (new) The apparatus of claim 27, wherein the digital phase locked loop further comprises a numerically-controlled oscillator, a fourth divider, a phase comparator and a low-pass filter for producing a locally generated reference clock signal.

34. (new) The apparatus of claim 27, wherein a selection mode is implemented to choose the local 8 KHz frequency from the first or the second divider as a reference for a phase comparator.

35. (new) The apparatus of claim 33, wherein the numerically-controlled oscillator is implemented as third divider that is a $Y_2/2^{N}{}_2$ that receives the high speed bus clock signal.

36. (new) The apparatus of claim 33, wherein the fourth divider is implemented as a $1/N_3$ divider that receives the output of the numerically controlled oscillator to produce a locally generated reference signal.

37. (new) The apparatus of claim 33, wherein phase comparator compares a time delay between rising edges of the external reference clock and a locally generated reference clock to determine a phase error as a correction factor to modify the value of Y_2.

38. (new) The apparatus of claim 36, wherein the value of N_3 in the $1/N_3$ divider is chosen from a group of integers including 256, 193 or 192 depending on the numerically-controlled oscillator clock output.

39. (new) The apparatus of claim 37, wherein the value of Y_2 is increased, when the external reference clock frequency edge occurs before the locally generated reference clock frequency edge.

40. (new) The apparatus of claim 37, wherein the value of Y_2 is decreased, when the external reference clock frequency edge occurs after the locally generated reference clock frequency edge.

42. (new) The apparatus of claim 39, wherein the value of Y_2 is increased by an amount proportional to the difference in time between the external reference clock frequency edge and the locally generated reference clock frequency edge.

43. (new) The apparatus of claim 40, wherein the value of Y_2 is decreased by an amount proportional to the difference in time between the external reference clock frequency edge and the locally generated reference clock frequency edge.

AMENDMENTS TO THE DRAWINGS:

The attached sheets of drawings includes changes to Figures 1, 2 and 3. These sheets, replaces the original sheets including.

Applicant believes that changes made to drawings do not add new matter, the changes are commensurate with either the minor changes made to the specification, or matter that was in the original disclosure.

In amended Figure 1, the lower portion of the box marked 110, has been divided into two parts and marked 110(a) and 110(b) to point out that 110(a) and 110(b) are two registers to control the operation as disclosed in the following paragraph

"In yet another embodiment of the present invention, and in reference to Figure 1, The network timing recovery (NTR) method and apparatus 100, contains two registers 110a and 110b to control its operation. The NTR_CSR (Control and Status Register) is split notionally into a 16-bit control register (bits 15:0) and a 16-bit status register (bits 31:16), though not all these bits are actually used"

In amended Figure 2, divider 208 is marked $Y_2/2^{N}{}_2$, in replacing the marking from Y/2N, to differentiate it from Y divider 150 of Figure 1, and divider 212 is marked $1/N_3$ to differentiate it from N divider 140 of Figure 1.

In amended Figure 3, Y is replaced by Y_1 in blocks 330, 335 and 340 and N is replaced by N_1 in blocks 315 and 340, so as differentiate those from the N dividers and Y dividers of NTR of the current invention.